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58-25265 Feb. 15, 1983 L6: 1 of 1

MANUFACTURE OF MOSFET

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ASSIGNEE: SANYO DENKI KK
APPL NO: 56-123799
DATE FILED: Aug. 6, 1981
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INT-CL: H01L 29/78; //H01L 21/316; H01L 29/62.

ABSTRACT:

PURPOSE:To improve the characteristic of MOSFET by making a source and a drain by using as a mask a poly-Si gate electrode provided on a P type Si substrate through the intermediary of a gate insulated film, by applying high-pressure low-temperature oxidation processing thereto, by exposing poly-Si selectively, and by applying a large amount of doping thereto.

CONSTITUTION:A poly-Si gate electrode 3 is prepared on a P type Si substrate 1 through the intermediary of a gate oxide film 2, and an N type soource 4 and an N type drain 5 are prepared by P diffusion with the electrode 3 as a mask. When they are oxidized subsequently in an atmosphere of high pressure and low temerature, an oxide film 6 on the poly-Si electrode 3 is made thinner than an oxide film 7 on the Si substrate. Next, the poly-Si oxide film 6 is removed selectively and P diffusion is conducted under the condition that the oxide film 7 of the substrate remains. Thereby only the poly-Si 3 is doped much and made to be of low resistance. This constitution enables lowering of a resistance value of the gate electrode of MOSFET wherein the depth of junction of the source and drain and the thickness of the gate oxide film are small, and thus the characteristic thereof can be improved.
=>

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(全 2 頁)

(54)MOSFETの製造方法

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(21)特願 昭56—123799
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明細書

1. 発明の名称 MOS FETの製造方法

2. 特許請求の範囲

1) 一導電型半導体基板表面にゲート絶縁膜を介して多結晶シリコンから成るゲート電極を形成し、このゲート電極をマスクとして上記基板に逆導電型の不純物を導入してソース、ドレインを設け、次に高圧水蒸気酸化雰囲気中でゲート電極を形成している多結晶シリコンと上記ソース、ドレインとを酸化して多結晶シリコン上に比較的厚い多結晶酸化膜とソース、ドレイン表面に比較的薄い基板酸化膜とを形成し、続いて基板酸化膜は残存させた状態で多結晶酸化膜を除去して多結晶シリコンを露出し、最後にこの露出多結晶シリコンの表面から不純物を多量にドープしてゲート電極としての抵抗値を下げる事を特徴としたMOS FETの製造方法。

3. 発明の詳細な説明

本発明はMOS FETの製造方法に関し、特に多結晶シリコンをゲート電極としたセルフアライン法を応用した方法を提供するものである。

最近のMOS FETの微細チャンネル化に伴い、ソース、ドレインの接合深さは浅く、またゲート酸化膜も薄くする必要がある。

接合深さを浅くしようとする結果、従来のP_2O_5のプレデポジション法でソース、ドレインをセルフアラインすると、ゲート電極を構成する多結晶シリコンへの導入不純物が不足してゲート電極の抵抗値が高い値となり、FETとして使用出来ない。またイオン注入法によってソース、ドレインを形成する場合は、その注入後にゲート酸化膜をマスクとしてP_2O_5をプレデポジション法を用いて多結晶シリコンの抵抗値を下げる事は可能であるが、ゲート酸化膜が薄く設定されているのでP_2O_5の拡散マスクとしての機能を果さなくなる。

本発明はこのような問題点に鑑みて為されたものであって、以下に図面を参照しつつ詳述する。

第1図は一導電型半導体基板、例えばP型のシリコン基板(1)上にゲート酸化膜(2)を介して多結晶シリコンから成るゲート電極(3)を設けた状態を示

している。

次にこのゲート電極(3)をN型不純物の拡散に対するマスクとしてN型の不純物、例えばP_2O_5をプレデポジション法等を用いて拡散してN型のソース、ドレイン(4)(5)を形成する（第2図）。

引き続いてこの第2図に示す状態の基板を高圧低温雰囲気中で酸化し、多結晶シリコンから成るゲート電極(3)並びにソース、ドレイン(4)(5)表面を酸化する。この高圧低温酸化に依ると、多結晶シリコン表面に成長する酸化膜の厚みと、単結晶シリコン表面に形成される酸化膜の厚みが相違し、前者の方が後者より薄い。具体例を挙げて説明すると、750℃で6kg/cm²、スチーム酸化を40分間施すと、第3図に示す如く、多結晶シリコン(3)表面には約1400Åの多結晶酸化膜(6)が、またソース、ドレイン(4)(5)表面には約2500Åの基板酸化膜(7)が夫々成長する。

次に通常のRIEエッチング法で多結晶酸化膜(6)及び基板酸化膜(7)をエッチングするのであるが、[illegible]が除去された時点で終了する必要がある。このRIEエッチング法の場合、多結晶酸化膜(6)のエッチングレートも基板酸化膜(7)のそれも同じであるので、比較的膜厚の薄い多結晶酸化膜(6)が除去された時点でも基板酸化膜(7)は第4図に示す如く1000Å程度残存している。1000Å程度の厚みの酸化膜は通常一般に行われているP_2O_5のプレデポジション法に依る拡散に対する遮蔽効果を有しているので、第4図の状態の基板(1)にP_2O_5のプレデポジション法に依る拡散を行うと多結晶シリコンから成るゲート電極(3)にのみ多量の燐が拡散され、該電極(3)の抵抗値を下げる事が出来る。

本発明は以上の説明から明らかな如く、高圧低温酸化での多結晶シリコンと単結晶シリコンとの酸化膜の成長速度の違いを用いてゲート電極にのみ不純物を拡散しているので、ソース、ドレインの接合深さが浅く、ゲート酸化膜の厚みの薄いMOS FETのゲート電極の抵抗値を下げる事が出来、特性の良く揃ったMOS FETの製造が可能となる。

4. 図面の簡単な説明

第1図乃至第4図は本発明方法を工程順に示した断面図であって、(1)は基板、(2)はゲート酸化膜、(3)はゲート電極、(4)(5)はソース、ドレイン、(6)は多結晶酸化膜、(7)は基板酸化膜、を夫々示している。

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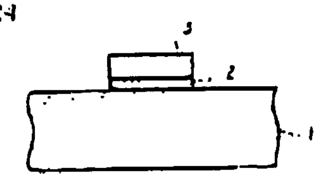
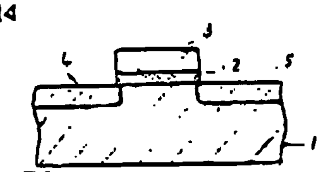
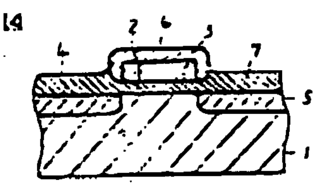
第1図



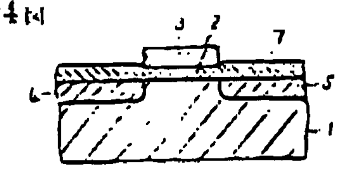
第2図



第3図



第4図



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(54) Method of manufacturing MOS FET

(21) Patent application: Sho.56(1981)-123799

(22) Applied for: 8/6/1981

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Specifications

1. Name of Invention: Method of MOS FET manufacture

2. Scope of Patent Application:

1) A method of manufacturing a MOS FET characterized by forming a gate electrode made of polycrystalline silicon through the intermediation of gate insulating film on the surface of a conductive type semiconductor substrate, introducing impurities of the inverse conductive type on the above substrate with this gate electrode as a mask, installing source and drain areas, and next, in a high-pressure low-temperature oxidizing atmosphere, oxidizing the above source and drain and the polycrystalline silicon that forms the gate electrode, and forming both a relatively thin polycrystalline silicon oxidized film on the polycrystalline silicon and a relatively thick oxidized substrate

film on the source and drain surfaces, proceeding to remove the polycrystalline oxide film under conditions whereby the substrate's oxidized film is left on, exposing the polycrystalline silicon, and finally doping this exposed polycrystalline silicon surface with a large amount of impurity to lower its resistance values as a gate electrode.

3. **Detailed explanation of invention**

This invention is one bearing on a method for MOS FET manufacture and particularly one providing a method for applying the self-aligning method, making polycrystalline silicon the gate electrode.

With the short-channeling of recent MOS-FETs, there is a need to make the source and drain contact surfaces shallow and also to make the gate oxide film thin.

A result of trying to make the contact surfaces shallow, when one has the source and drain self-align by the usual P_2O_5 predeposition method, the impurity introduced into the polycrystalline silicon forming the gate electrode is insufficient and the gate electrode's resistance values stay high and it cannot be used as a FET. Also, in making the source and drain using ion injection it is possible to reduce the polycrystalline silicon's resistance values by using the P_2O_5 predeposition method with the oxidized gate film as a mask after that injection; and yet since the gate oxide film is made thin, the function of the P_2O_5 as a diffusion mask will not be fulfilled.

This invention has been devised with such problem points in mind, and will be carefully described in relation to the figures.

Figure 1 shows the situation wherein gate electrode 3 made of polycrystalline silicon has been installed on a conductive type semiconductor substrate, for example, P-type silicon substrate 1 intermediated by gate oxidized electrode 2.

Next, in Figure 2, we form N-type source 4 and drain 5 by diffusing such an N-type impurity as P_2O_5 by the predeposition method with this as a mask for the N-type impurity diffusion on this gate electrode 3.

Going on, we do oxidation on the substrate under the conditions shown in Figure 2 in a high-pressure low-temperature atmosphere, and oxidize gate electrode 3 made of polycrystalline silicon, as well as gate electrode 3 and the source 4 and drain 5 surfaces. By doing this high-pressure low-temperature oxidation, the thickness of the oxide film deposited on the polycrystalline silicon surface differs from the thickness of the oxide film formed on the monocrystalline silicon surface. The former is thinner than the latter.

To explain a specific case, when we do steam oxidation at 750°C and 6kg/cm² for 40 minutes, polycrystalline oxide film 6 of about 1400Å is deposited on the surface of polycrystalline silicon 3, and substrate oxide film 7 of about 2500Å is deposited on the surfaces of source 4 and drain 5, as shown in Figure 3.

Next is the etching of polycrystalline oxide film 6 and substrate oxide film 7 by ordinary BHF etching. This etching process is important and must be concluded by the time that polycrystalline oxide film 6 has been removed. With this BHF etching method, because the etching rates for polycrystalline oxide film 5 and for substrate oxide film 7 are the same, substrate oxide film 7 of some 1000Å remains, as in Figure 4, even after relatively thin polycrystalline oxide film 6 is removed.

The oxide film of some 1000Å thickness has a [illegible] effect on the diffusion by P_2O_5 predeposition ordinarily and generally done, so that when predeposition-method diffusion is done on substrate 1 under the conditions of Figure 4, a large amount of phosphorus is diffused only on gate electrode 3 which is made of polycrystalline silicon, and the resistance values of the said electrode 3 can be reduced.

As is clear from the above explanation, because this invention diffuses the impurity only on the gate electrode, using the difference in deposition speed of the oxide films on the monocrystalline silicon and polycrystalline silicon in high-pressure /low temperature oxidation, the contact depth of the source and drain is shallow, and the resistance values of the MOS FET gate electrode with its thin gate oxide film can be reduced, making possible the manufacture of a specially fine MOS FET.

4. Simple explanation of figures

Figures 1 to 4 are cross-sectional diagrams showing the method of this invention by its processing sequences.

1 ..... substrate
2 ..... gate oxide film
3 ..... gate electrode
4, 5 ... source, drain
6 ..... polycrystalline oxide film
7 ..... substrate oxide film

Applicant: Sanyo Electric Co., Ltd.

Agent: Shizuo Sano, Patent attorney